CLAIMS

What is claimed is:

1. A transmitter coupled to at least two single-channel links of a high-bandwidth link, the transmitter comprising:

at least two registers each associated with a single channel link and each receiving a portion of user data provided to the transmitter from a module; and

a framer providing i) the user data from the module as a packet having a packet delineator and based on a packet format, and ii) the packet delineator on a particular single-channel link; and

wherein one register provides a portion of the packet with the packet delineator to a particular single-channel link, and each register provides a corresponding portion of the packet to an associated single-channel link.

2. The invention as recited in claim 1, wherein, for a sequence of packets, the transmitter inserts inter-packet fill to provide the packet delineator of each packet on the particular single-channel link.

3. The invention as recited in claim 1, wherein at least one single-channel link is a serial link.

4. The invention as recited in claim 3, wherein the serial link is an 8B/10B encoded link operating in accordance with either a Ethernet standard, a Fibre-channel standard, or a Infiniband standard.

5. The invention as recited in claim 3, wherein the serial link applies scrambling to the packet including the user data.

6. The invention as recited in claim 3, wherein the serial link operates in accordance with a SONET standard.

7. The invention as recited in claim 1, wherein the at least two single-channel links are parallel links.

8. The invention as recited in claim 7, wherein the parallel links operate in

accordance with either a PCI bus standard or a RapidIO standard.

9. The invention as recited in claim 1, wherein the transmitter operates in a node in accordance with an asynchronous transfer mode standard or a synchronous optical network standard.

10. The invention as recited in claim 1, wherein the transmitter is embodied in an integrated circuit.

11. A receiver generating user data for a module from a packet received from at least two single-channel links forming a high-bandwidth link, the receiver comprising:

at least two registers each receiving a portion of the packet, wherein

one register provides a portion of the packet with a packet delineator from a particular single channel link, and each register provides a corresponding portion of the packet from an associated single-channel link; and

a framer that 1) forms the packet from the packet delineator and 2) extracts the user data based on a packet format.

12. The invention as recited in claim 11, wherein the packet format includes information in at least one message channel other than the user data.

13. The invention as recited in claim 11, wherein the packet format includes error detection or error detection/correction information.

14. The invention as recited in claim 13, wherein the error detection or error detection/correction information is cyclic redundancy check information.

15. The invention as recited in claim 11, wherein the packet format allows for discarding of inter-packet fill.

16. The invention as recited in claim 11, wherein the apparatus operates in a node in accordance with an asynchronous transfer mode standard or a synchronous optical network standard.

17. The invention as recited in claim 11, wherein the circuit is embodied in an integrated circuit.

18. A method of transmitting user data from a module over at least two single-channel links of a high-bandwidth link, the method comprising the steps of:

(a) receiving, in each of at least two registers each having a corresponding single channel link, a portion of user data from the module; and

(b) providing 1) the user data as a packet having a packet delineator based on a packet format, and 2) the packet delineator on a particular single-channel link; and

wherein one register provides a portion of the packet with the packet delineator to a particular single-channel link, and each register provides a corresponding portion of the packet to an associated single-channel link.

19. The invention as recited in claim 18, wherein step (b) further includes the step of inserting inter-packet fill such that the packet delineator occurs on the particular single-channel link for each packet in a sequence of packets.

20. The invention as recited in claim 18, wherein, for step (b) at least one single-channel link is a serial link.

21. The invention as recited in claim 20, wherein, for step (b) the serial link is an 8B/10B encoded link operating in accordance with either a Ethernet standard, a Fibre-channel standard, or a Infiniband standard.

22. The invention as recited in claim 20, further including the step of scrambling at least one portion of the packet including the user data.

23. The invention as recited in claim 20, wherein, for step (b), the serial link operates in accordance with a SONET standard.

24. The invention as recited in claim 18, wherein, for step (b) the at least two single-channel links are parallel links.

25. The invention as recited in claim 18, wherein, for step (b) the parallel links operate in accordance with either a PCI bus standard or a RapidIO standard.

26. The invention as recited in claim 18, wherein the method is implemented within a node in accordance with an asynchronous transfer mode standard or a synchronous optical network standard.

27. The invention as recited in claim 18, wherein the method is implemented within a processor of an integrated circuit.

28. A method of generating user data for a module from a packet received from at least two single-channel links forming a high-bandwidth link, the method comprising the steps of:

(a) receiving, in each of at least two registers, a corresponding portion of the packet;

(b) providing 1) a portion of the packet with a packet delineator from a particular single channel link, and 2) a corresponding portion of the packet from an associated single-channel link;

(c) forming the packet from the packet delineator; and

(d) extracting the user data based on a packet format.

29. The invention as recited in claim 28, wherein step (d) extracts information in at least one message channel other than the user data.

30. The invention as recited in claim 28, wherein step (c) forms the packet based on error detection or error detection/correction information included with the packet in accordance with the packet format.

31. The invention as recited in claim 30, wherein the error detection or error detection/correction information is cyclic redundancy check information.

32. The invention as recited in claim 28, wherein step (c) discards inter-packet fill.

33. The invention as recited in claim 28, wherein the method is implemented within a node in accordance with an asynchronous transfer mode standard or a synchronous optical network standard.

34. The invention as recited in claim 28, wherein the method is implemented within a processor of an integrated circuit.